GP 2763

Docket No.: M-1007-6C US

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FACSIMILE: (408) 453-7979

25 METRO DRIVE, SUITE 700
San Jose, California 95110
(408) 453-9200

September 21, 1999

Box Non-Fee Amendment
Assistant Commissioner For Patents
Washington, D.C. 20231

Re:
Applicant: Amr M. Mohsen
Assignee: Aptix Corporation
Title: FIELD PROGRAMMABLE PRINTED CIRCUIT BOARD
Serial No.: 08/632,298 Filed: April 12, 1996
Examiner: H. Jones Group Art Unit: 2763
Docket No.: M-1007-6C US

Sir:

Transmitted herewith are the following documents in the above-identified application:

(1) Return Receipt Postcard;
(2) This Transmittal Letter (in duplicate); and
(3) Response (12 pages)

☒ No additional fee is required.
☐ The fee has been calculated as shown below:

CLAIMS AS AMENDED

	Claims Remaining *After* Amendment		Highest No. Previously Paid For		Present Extra		Rate		Additional Fee
Total Claims	22	Minus	58	=	0	x	$18	$	0.00
Independent Claims	6	Minus	12	=	0	x	$78	$	0.00

☐ Fee of for the first filing of one or more multiple dependent claims per application $

☐ Fee for Request for Extension of Time $

Total additional fee for this Amendment: $ 0.00

☒ Conditional Petition for Extension of Time: If an extension of time is required for timely filing of the enclosed document(s) after all papers filed with this transmittal have been considered, an extension of time is hereby requested.

☒ Please charge our Deposit Account No. 19-2386 in the amount of $ 0.00

☒ Also, charge any additional fees required and credit any overpayment to our Deposit Account No. 19-2386.

Total: $ 0.00

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner For Patents, Washington, D.C. 20231, on September 21, 1999.

Ronald J. Meetin
Attorney for Applicant(s)

21 Sep. 1999
Date of Signature

Respectfully submitted,

Ronald J. Meetin

Ronald J. Meetin
Attorney for Applicant
Reg. No. 29,089

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#22
10-21

Applicant:	Amr M. Mohsen		
Assignee:	Aptix Corporation		
Title:	FIELD PROGRAMMABLE PRINTED CIRCUIT BOARD		
Serial No.:	08/632,298	Filed:	04/12/96
Examiner:	H. Jones	Group Art Unit:	2763
Docket No.:	M-1007-6C US		

San Jose, California
September 21, 1999

BOX NON-FEE AMENDMENT
ASSISTANT COMMISSIONER FOR PATENTS
Washington, D. C. 20231

RESPONSE

Sir:

The following remarks are submitted in response to the Office Action mailed 22 June 1999 for the above patent application.

Claims 20 - 28, 37 - 39, 42, 50 - 52, and 72 - 77 have been rejected under the obviousness-type double-patenting doctrine as unpatentable over Claims 1 - 17 of U.S. Patent 5,377,124. The Examiner states that the "nonstatutory double-patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the 'right to exclude' granted by a patent and to prevent possible harassment by multiple assignees." This rejection is respectfully traversed.

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

The Examiner has indicated that a suitable terminal disclaimer would overcome a non-statutory double-patenting rejection. However, Applicant's attorney believes that a terminal disclaimer is not needed to overcome the present non-statutory double-patenting rejection.

U.S. Patent 5,377,124 issued 27 December 1994 on an application filed 20 September 1989. Both of these dates are prior to 8 June 1995, the date on which the 1994 amendments to the U.S. Patent law came into effect for changing the term of a U.S. patent from seventeen years from the date of issue to twenty years from the earliest effective U.S. filing date of the application for patent, subject to certain transitional provisions that are not relevant here. Accordingly, U.S. Patent 5,377,124 expires seventeen years after its issue date. Since U.S. Patent 5,377,124 issued 27 December 1994, U.S. Patent 5,377,124 expires 27 December 2011.

The present application was filed 12 April 1996 as a continuation of an application filed, in turn, as a continuation of the application which was filed 20 September 1989 and issued as U.S. Patent 5, 377,124. Inasmuch as the 12 April 1996 filing date of the present application is subsequent to 8 June 1995, a patent granted on the present application will expire twenty years from the earliest effective filing date of the present application. The earliest effective filing date of the present application is 20 September 1989. Consequently, a patent granted on the present application will expire 20 September 2009.

The 27 December 2011 expiration date of U.S. Patent 5,377,124 is later than the projected 20 September 2009 expiration date for a patent granted on the present application. Hence, a patent granted on a present application will expire prior to the expiration of U.S. Patent 5,377,124 and cannot timewise extend the exclusionary right provided by U.S. Patent 5,377,124. Grounds for the present non-statutory double-patenting rejection are not present

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SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

here. Accordingly, the non-statutory double-patenting rejection of Claims 20 - 28, 37 - 39, 42, 50 - 52, and 72 - 77 should be withdrawn.

As a separate matter, a determination has not yet been made as to what subject matter is allowable in the present application but for the double-patenting rejection. Even if the Examiner should feel that the double-patenting rejection is appropriate in the present circumstances, Applicant's attorney is not currently in a position to determine whether to submit a terminal disclaimer or to further contest the double-patenting rejection. Accordingly, should the Examiner maintain the double-patenting rejection, Applicant's attorney respectfully requests that the double-patenting rejection be placed in abeyance until all the allowable subject matter has been ascertained.

Claims 20 - 28, 37 - 39, 42, 50 - 52, and 72 - 77 have been rejected under 35 USC 102(a) as anticipated by the article in the IBM Technical Disclosure Bulletin ("IBM TDB"). This rejection is respectfully traversed.

The IBM TDB article discloses a chip interconnection structure in which chips (integrated circuits) 2 mounted over a wiring wafer 1 are interconnected by way of a two-dimensional grid of wires provided over wafer 1. As shown in Fig. 2 of the IBM TDB article, each horizontal or vertical wire provided over wafer 1 appears to consist of, or be divided into, multiple wiring segments 3. Switches 4 are utilized to selectively interconnect wiring segments 3, thereby enabling chips 2 to be interconnected in a desired manner.

Independent device Claims 20, 23, 37, and 42 each recite an interconnection structure in which at least one programmable interconnect chip ("PIC") or programmable integrated circuit (also "PIC") having two sets of conductive leads is utilized in interconnecting

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

electronic components connected to a board, such as a printed circuit board, or other such interconnection substrate.

A major difference between the interconnect structure of the IBM TDB article and the interconnect structure covered by each of Claims 20, 23, 37, and 42 is that the programmable interconnect function is performed in a different location in the interconnect structure of the IBM TDB article than in the interconnect structure of each of Claims 20, 23, 37, and 42. The interconnect architecture covered by Claims 20, 23, 37, and 42 is fundamentally different from the interconnect architecture in the IBM TDB article.

More particularly, the programmable interconnect function in each of Claims 20, 23, 37, and 42 is performed in one or more PICs connected to a printed circuit board or other interconnect substrate to which electronic components are connected. The electronic components are programmably interconnected by suitably programming the one or more PICs.

In contrast, the programmable interconnect function in the IBM TDB article is performed in wiring wafer 1 on which chips 2 are mounted. The programmable interconnect function in the IBM TDB article is not performed in any chips mounted on, or otherwise connected to, wiring wafer 1. Nothing in the IBM TDB article discloses that certain of chips 2 are, or can be, programmed to programmably interconnect others of chips 2. The interconnect structure in the IBM TDB article lacks the PICs of Claims 20, 23, 37, and 42. Consequently, the IBM TDB article does not anticipate any of Claims 20, 23, 37, and 42.

Furthermore, nothing in the IBM TDB article would furnish a person skilled in the interconnection art with any motivation or insensitive for modifying the interconnection structure of the IBM TDB article to include one or more PICs that provide a programmable interconnection function of the type covered by Claims 20, 23, 37, and 42. Accordingly, the

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

IBM TDB article does not make any of Claims 20, 23, 37, and 42 obvious. Claims 20, 23, 37, and 42 are therefore patentable over the IBM TDB article.

Device Claims 21, 22, 24 - 28, 38, and 39 variously depend (directly or indirectly) from Claims 20, 23, and 37. Consequently, dependent Claims 21, 22, 24 - 28, 38, and 39 are variously patentable over the IBM TDB article for the same reasons as Claims 20, 23, and 37.

The IBM TDB article does not disclose the PIC-located transistor-based programming arrangement of dependent Claim 21 or 27. Dependent Claims 22 and 28 disclose a programming arrangement that can be referred to as an antifuse. The IBM TDB article does not disclose the antifuse programming arrangement of Claim 22 or 28. Nor does the IBM TDB article disclose the multi-layered board of dependent Claim 38. Claims 21, 22, 27, 28, and 38 are thus separately patentable over the IBM TDB article.

Dependent Claim 24 recites that pads are arranged in an area matrix so that at least one of the pads is internal to the pads along the periphery of the area matrix. The IBM TDB article does not disclose any internal pads and thus does not disclose or suggest the further limitation of Claim 24. Nor does the IBM TDB article disclose or suggest the specific area-matrix arrangements recited in Claims 25 and 26 which depend from Claim 24. Claims 24 - 26 are likewise separately patentable over the IBM TDB article.

Independent method Claim 50 is directed to the operation of a structure in which at least one PIC having two sets of conductive leads is connected to a substrate. The one or more PICs are programmable for programmably interconnecting electronic components connected to the substrate.

Similar to what was said above about device Claims 20, 23, 37, and 42, the interconnect structure of the IBM TDB article does not meet the requirement of method Claim

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

50 that the programmable interconnect function be performed in one or more PICs connected to a substrate. Hence, the IBM TDB article does not anticipate Claim 50. Nor would anything in the IBM TDB article make Claim 50 obvious to a person skilled in the interconnection art. Consequently, Claim 50 is patentable over the IBM TDB article.

Claims 51 and 52 depend from Claim 50. Accordingly, Claims 51 and 52 are patentable over the IBM TDB article for the same reasons as Claim 50.

Independent device Claim 72, which provides that a bus system electrically interconnects a group of PICs, is generally directed to application Fig. 3c in which PICs 321-1 through 321-6 are electrically interconnected through a bus system formed with central bus 323-10 and further buses 323-1 through 323-6. The IBM TDB article does not disclose the PIC/bus-system architecture of Claim 72. Hence, the IBM TDB article does not anticipate Claim 72.

Additionally, nothing in the IBM TDB article would lead a person skilled in the interconnection art to the PIC/bus-system architecture of Claim 72. Accordingly, Claim 72 is patentable over the IBM TDB article.

Device Claims 73 - 77 depend (directly or indirectly) from Claim 72 and thus are patentable over the IBM TDB article on the same basis as Claim 72.

The IBM TDB article does not disclose the multi-layer substrate feature of dependent Claim 73. This makes Claim 73 separately patentable over the IBM TDB article.

Dependent Claim 75 provides that the bus system comprises a central bus and a group of further buses that respectively connect the central bus to the PICs. The IBM TDB article does not disclose or suggest anything remotely similar to the bus architecture of Claim 75. Nor does the IBM TDB article disclose or suggest the further bus architecture limitation of

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SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

dependent Claim 76 or 77. Hence, Claims 75 - 77 are separately patentable over the IBM TDB article.

Claims 20 - 28, 37 - 39, 42, 50 - 52, and 72 - 77 have been rejected under 35 USC "102(e)" as anticipated by Kung et al ("Kung"). Presumably the Examiner means for this anticipation rejection to be under 35 USC 102(a) or 35 USC (b) rather than 35 USC 102(e) since Kung issued before the earliest effective filing date of the present application. In any event, the rejection is respectfully traversed.

Kung discloses an interconnection structure in which interconnection chips 10 are utilized to programmably interconnect electronic components such as processors and memories. Figs. 11A and 11B of Kung present examples of the interconnection structure.

As pointed out above, independent device Claims 20, 23, 37, and 42 each provide that electronic components connected to an interconnection substrate are programmably interconnected via at least one PIC having two sets of conductive leads. Claims 20, 23, 37, and 42 each further require that at least one lead in the two sets of conductive PIC leads comprise, or be divided into, two or more electrically separate conductive segments.

An explanation of what is meant by a conductive lead comprising, or being divided into, two or more electrically separate conductive segments is presented on page 7 of the Amendment dated 1 March 1999. For the Examiner's convenience, that explanation is repeated here:

> Insofar as what is meant by a lead comprising, or being divided into, two or more electrically separate conductive segments, note that Claims 20, 23, 37, and 42 each provide (a) that the conductive leads in one set of the conductive leads extend in one direction and (b) that the conductive leads in the other set of conductive leads extend in another direction not parallel to the first-mentioned direction. Hence, the electrically separate segments of each segmented conductive lead are situated largely in a straight line with one another. A pair of laterally separated conductive leads extending parallel to (but not in line with) each other, or a pair of conductive leads

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SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

meeting or crossing each other, are not electrically separate segments of a conductive lead as provided in Claims 20, 23, 37, and 42.

As pointed out on pages 7 and 8 of the 1 March 1999 Amendment, application Fig. 6b illustrates an example of the present programmable interconnect structure in which certain of the conductive leads in a PIC are segmented in the manner prescribed in Claims 20, 23, 37, and 42. Horizontal conductive lead 608-1 in PIC 605 of Fig. 6b consists of at least two electrically separate conductive segments. Short line 618-1 indicates one end of one segment of horizontal lead 608-1. Short lines 618-1 and 618-2 indicate the opposite ends of another segment of horizontal lead 608-1. As shown in Fig. 6b, these two segments of horizontal lead 608-1 of PIC 605 are situated in a straight line with one another. Likewise, the two electrically separate conductive segments of vertical conductive lead 609-1 in PIC 605 of Fig. 6b are situated in a straight line with one another.

An explanation of the advantages for using segmented PIC leads is presented on pages 8 and 9 of the 1 March 1999 amendment. This explanation is largely repeated in the following four paragraphs with suitable modifications to emphasize that the segmented leads are utilized in a PIC.

By furnishing at least one PIC of a programmable interconnect structure with at least one segmented programmable conductive lead as specified in Claim 20, 23, 37, or 42, the different segments of the programmable lead can be programmed to provide multiple interconnect functions rather than just one interconnect function as occurs with a non-segmented programmable conductive lead. This increases the flexibility and efficiency in implementing circuit designs using the programmable interconnect structure of the invention. Because the conductive PIC leads are utilized more efficiently, the total number of conductive PIC leads can be reduced. The PIC area can be reduced, thereby reducing the fabrication cost.

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

The interconnect function provided by each segment of a segmented programmable conductive lead of a PIC typically extends over a shorter distance than the interconnect function provided by an unsegmented programmable conductive lead. Consequently, the trade-off for increasing the number of available interconnect functions by utilizing one or more segmented programmable conductive leads is that the interconnect functions provided by the segments of each segmented PIC lead are typically shorter than interconnect functions provided by unsegmented programmable conductive leads.

Many circuit designs need some number of full-length interconnect functions. Accordingly, the selection of the number of programmable conductive leads that are to be implemented as segmented PIC leads depends on the typical types of circuit designs to be implemented with the programmable interconnect structure of the invention. As stated in the middle paragraph of page 18 of the specification in regard to the multi-cell configuration of application Fig. 6b,

> The particular configuration of the conductive leads extending across one cell and from that cell to adjacent cells depends upon an analysis of the electrical functions to be carried out by the programmable printed circuit board and is selected using the most probable types of system requirements to be imposed on programmable interconnect chip 605. This selection depends upon an analysis of the circuit functions to be performed by the programmable printed circuit board of this invention and thus the actual configuration of the programmable interconnect chip is determined in light of the proposed uses for the programmable printed circuit board.

Also, each segment of a segmented conductive PIC lead has less capacitance than an otherwise equivalent full-length conductive lead. With the capacitive loading reduced, higher operational speed can be achieved. In short, utilization of segmented conductive leads in at

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SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

least one PIC of the present programmable interconnect structure enables the speed and efficiency to be increased while simultaneously enabling the cost to be reduced.

As far as Applicant's attorney can determine, Kung does not disclose that any of interconnection chips 10 contains a segmented lead. For example, consider interconnection chip 10c in Fig. 4 of Kung. Taking note of the fact that each of Claims 20, 23, 37, and 42 provides that at least one PIC has a first set of conductive leads extending in a first direction and a second set of conductive leads extending in a second direction different from the first direction, interconnection chip 10c is the only one of Kung's interconnection chips 10 illustrated as having one set of leads extending in one direction and another set of leads extending in another direction. To the extent that the leads shown in Fig. 4 of Kung may generally represent the actual physical configuration of those leads, none of the leads in interconnection chip 10c is segmented in the manner required by Claim 20, 23, 37, or 42. Kung thus does not anticipate any of Claims 20, 23, 37, or 42.

Additionally, nothing in Kung would provide a person skilled in the interconnection art with a suggestion to incorporate one or more segmented leads into any of Kung's interconnection chips 10. Nowhere does Kung deal with the problems which, as described above, are overcome with segmented leads. In particular, Kung does not indicate any concern with enhancing the internal interconnect capability of a chip 10 in any way remotely similar to what is achieved by the lead segmentation prescribed in Claims 20, 23, 37, and 42. For these reasons, Kung does not make any of Claims 20, 23, 37, and 42 obvious. Consequently, Claims 20, 23, 37, and 42 are patentable over Kung.

Kung does not disclose the transistor-based programming arrangement of dependent Claim 21 or 27, the antifuse programming arrangement of dependent Claim 22 or 28, the

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

internal-pad limitation of dependent Claim 24, the specific area-matrix arrangements of dependent claims 25 and 26, or the multi-layered board of dependent Claim 38. Consequently, Claims 21, 22, 24 - 28, and 38 are separately patentable over Kung.

Dependent device Claims 21, 22, 24 - 28, 38, and 39 are patentable over Kung on the same basis as Claims 20, 23, and 37.

Turning to independent method Claim 50, it requires that at least one lead in the two sets of conductive PIC leads be a segmented lead. Inasmuch as Kung does not disclose that any of interconnection chips 10 contains a segmented lead, Kung does not anticipate Claim 50. For the reasons presented above in connection with Claims 20, 23, 37, and 42, nothing in Kung would make Claim 50 obvious. Hence, Claim 50 is patentable over Kung.

Dependent method Claims 51 and 52 are patentable over Kung on the same basis as Claim 50.

Independent device Claim 72 specifies that a bus system electrically interconnects a group of PICs. As far as Applicant's attorney can determine, Kung does not disclose the use of a bus system for interconnecting interconnect chips 10. For example, consider Figs. 11A and 11B of Kung. While Figs. 11A and 11B illustrate interconnection chips 10 as being interconnected, the interconnection of chips 10 in Fig. 11A and 11B is performed directly and not through a bus system. Kung thus does not anticipate Claim 72.

Furthermore, nothing in Kung would lead a person skilled in the interconnection art to the PIC/bus-system architecture of Claim 72. For example, it would be totally illogical to substitute a bus system for any interconnect chip 10 in Fig. 11A or 11B of Kung. Claim 72 is therefore patentable over Kung.

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

Dependent device Claims 73 - 77 are patentable over Kung on the same basis as Claim 72.

Kung does not disclose the multi-layer substrate feature of dependent Claim 73. Nor does Kung disclose or suggest anything remotely similar to the particular bus architecture of dependent Claim 75. Kung does not disclose or suggest the further bus architecture limitation of dependent Claim 76 or 77. For these reasons, Claims 73 and 75 - 77 are separately patentable over Kung.

In summary, the double-patenting rejection has been shown to be inappropriate. Claims 20 - 28, 37 - 39, 42, 50 - 52, and 72 - 77 have been shown to be patentable over the applied art. Accordingly, Claims 20 - 28, 37 - 39, 42, 50 - 52, and 72 - 77 should be allowed so that the application may proceed to issue.

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on September 21, 1999.

Ronald J. Meetin — 21 Sep. 1999

Attorney for Applicant(s) — Date of Signature

Respectfully submitted,

Ronald J. Meetin

Ronald J. Meetin
Attorney for Applicant
Reg. No. 29,089

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979